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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/761,239	CHOI, JONG-HYUN	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Apr 24, Jun 25, and Jul 17, 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,10-13,16-24,26,29-33 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-24, 26, and 29-31* is/are allowed.

6)☒ Claim(s) *1-3,10-13,16-18,32,33 and 35-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/RCE

The amendments submitted on Apr 24, 2008 and Jul 17, 2008; and the RCE submitted on Jun 25, 2008 have been reviewed and considered with the following results:

The RCE was approved, allowing the Jul 17th amendment to entered and considered.

The cancellation of claims 6 rendered its rejection moot.

The amended claims overcame the objections to claims 19-24, 26, 32-33, and 35-37 described on page 3 of the previous Office Action. Therefore, those objections have been withdrawn.

Amended claims 10 and 29 overcame the rejections of claims 10-13, 16-18 and 29-31 under 35 U.S.C. 112 as described on pages 3-4 of the previous Office Action. Although those previous rejections have now been withdrawn, amended claim 10 created a new concern with respect to claim 16, which is described later under the appropriate section.

Amended claims 1, 10, and 32, and/or some of the arguments, overcame most of the prior art rejections described on pages 4-12 of the previous Office Action. Therefore, the following rejections have been withdrawn: 1) claims 1-3, 10-13, and 16-18 under 35 U.S.C. 103(a), with respect to Hardee/Amanai; and 2) claims 1-3, 10-13, 16, 32-33 and 35-37 under 35 U.S.C. 103(a), with respect to Wright et al./Amanai. The reference of Wright does not show or disclose the second and third transistors having substantially the same gate insulation layer thickness as now cited within independent claims 1, 10, and 32. However, the previous rejections of claims 1-3, 10-13, and 16-18 using the Hardee and Amanai references have been modified to address the limitations, with respect to the claimed inverter and its transistors, and the applicant's

arguments/comments. These modified rejections, as well as rejections of claims 32-33 and 35-37, are described later under the appropriate section. Related comments are described later under the Response to Arguments section.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 16 is now rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear how the inverter's PMOS and NMOS transistors, and the "another voltage", cited within claim 16 relate to the "NMOS and PMOS transistors" and "third voltage" now cited within claim 10. For example, are they meant to refer to the same transistors and voltage, or to other distinct transistors and voltage?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 10-13, 16-18, 32-33, and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hardee, in view of Amanai and Wang et al. (Wang), wherein the Hardee and Amanai references had both been cited in rejections of the previous Office Action, and the reference of Wang was previously cited on paper number 20070109. [Wang's reference provides an example of an inverter with PMOS and NMOS transistors, each having a thick gate insulation

layer.] One of ordinary skill in the art would understand that Fig. 1 of Hardee shows a level shifting type device for receiving an input signal alternating between 0V and VCC, and for effectively providing a corresponding output signal that will selectively alternate between 0V and VCCP. The device comprises first internal circuit 12, including first MOS transistor 12, operating at first voltage VCCP higher than power supply voltage VCC of the device (e.g. see column 1, lines 25-28); second internal circuit 16, including second MOS transistor 16 with a thin gate insulation layer (i.e. THIN OXIDE), operating at second voltage VCC lower than first voltage VCCP; and restricting means 14, including third MOS transistor 14 also having a thin gate insulation layer (i.e. THIN OXIDE), and operating at second voltage VCC, wherein restricting means 14 will restrict a voltage transmitted from first internal circuit 12 to second internal circuit 16 by applying the voltage from first internal circuit 12 to second internal circuit 16 through third MOS transistor 14. Although second MOS transistor 16 is controlled by the input signal alternating between VCC and 0V, this signal is neither clearly shown nor disclosed as being related to a row address signal in a memory device, nor is an inverter, with thick gate insulation layers shown coupled to the output. One of ordinary skill in the art would understand Hardee's device would be capable of operating with a row address signal as its input signal. Column 1, lines 24-28 of Hardee disclose the device relates to memory devices which may require the higher voltage, and therefore could be used with a memory device and its related signals. Amanai shows and discloses a memory related device utilizing a row address signal and a level shifter. For example, Fig. 1 of Amanai shows level shifter 15 controlled by a row address signal provided through gate 13. Therefore, it would have been obvious to one of ordinary skill in the art to supply second MOS transistor 16 of Hardee with a row address signal in a memory

device, and/or to replace Amanai's cross coupled level shifting type circuitry 15 with two of Hardee's level shifting devices (two are required to respond to, and provide, complementary type signals to correspond to Amanai's complementary inputs and outputs), wherein Hardee's second MOS transistor 16 would be controlled by at least one row address signal through Amanai's logic gate 13. [Note: Hardee's transistor 16 would receive the row address signal since it is the transistor receiving the alternating input signal. Transistor 14 receives VCC as its bias voltage.] The type of signal applied to Hardee's second MOS transistor would actually depend on what type of input signal is to be shifted to provide a higher "high" level output. Wang shows inverter P5,N5, in Figs. 4 and 5, receiving an output from series coupled transistors that include both thick and thin gate insulation layer transistors. Since inverter P5,N5 operates at VDDQ, a higher voltage than power supply VDD, both transistors P5 and N5 are shown with thick gate insulation layer transistors. Therefore, it would have been obvious to one of ordinary skill in the art to couple an inverter, such as Wang's P5,N5, to an output connection node between the first and third MOS transistors (i.e. 12 and 14, respectively) of Hardee, wherein the inverter would drive a word line in the memory device, rendering claim 1 obvious. The inverter would provide an inverted version of the output signal from Hardee's circuit, if it was desired or required, and also provide one means for isolating the word line from Hardee's device. The use of an inverter with PMOS and NMOS transistors each having a thick gate insulation layer would ensure the inverter's configuration corresponds to MOS transistor 12 of Hardee's device, thus allowing the transistors to have similar fabrication processes and operating characteristics, and ensure both transistors in the inverter can withstand the higher voltage VCCP. Since first MOS transistor 12 has a thick gate insulation layer (i.e. THICK OXIDE), and second MOS transistor 16 has a thin

gate insulation layer (i.e. THIN OXIDE), it would be obvious to one of ordinary skill in the art that the voltage transmitted from first internal circuit 12 to second internal circuit 16 would help reduce an electric field applied to the gate insulation layer of second MOS transistor 16 since restricting means 14 functions at a resistance device that provides a voltage drop across it, thus rendering claim 2 obvious. Second voltage VCC is a power supply voltage that would be either an external power supply voltage, or an internal power supply voltage, for the device, and claim 3 is rendered obvious. Interpreting Hardee's Fig. 1 circuit in a slightly different manner, the device comprises an output terminal (i.e. the unlabeled connection between transistors 12 and 14) selectively receiving high voltage VCCP higher than power supply voltage VCC of the device; first transistor 12 having a drain coupled to the output terminal, a source coupled to high voltage VCCP (which corresponds to a high power terminal receiving the high voltage), a gate coupled to a first input signal that selectively alternates between 0V and VCCP, and a thick gate insulation layer (i.e. THICK OXIDE); second transistor 14 having a drain coupled to the output terminal, a gate coupled to low voltage VCC lower than high voltage VCCP, and a thin gate insulation layer (i.e. THIN OXIDE); and third transistor 16 having a drain coupled to the source of second transistor 14, a source coupled to a ground voltage, a gate coupled to a second input signal selectively alternating between 0V and VCC, and a thin gate insulation layer (i.e. THIN OXIDE). For the same type of reasoning as described above with respect to claim 1, the second input signal applied to the gate of third transistor 16 is capable of being, or with respect to Amanai can be, a row address signal from a memory device, and an inverter (e.g. with PMOS and NMOS transistors P5 and N5 of Wang, with each transistor having a thick gate insulation layer) for driving a word line of a memory could obviously be coupled to a connection node of

the first and second transistors as now cited within claim 10. Therefore, claim 10 is rendered obvious. Since second voltage VCC is the power supply voltage, which is an external power supply voltage, or an internal power supply voltage, of the device, claim 11 is also rendered obvious. One of ordinary skill in the art would understand that 0V is a low level corresponding to the ground voltage. Therefore, the first input signal is selectable as one of a high level of high voltage VCCP and a low level of ground; and the second input signal is selectable as one of a high level of low voltage VCC and a low level of ground, rendering claims 12-13 obvious. Since inverter P5,N5 of Wang includes PMOS transistor P5 and NMOS transistor N5, with each transistor operating at voltage VCCP (of Hardee), which is higher than power supply voltage VCC (of Hardee), and each transistor has a thick gate insulation layer, claim 16 is rendered obvious. Hardee discloses that any number of NMOS transistors can be coupled in series to configure the switching circuit into a NAND logic configuration (e.g. see column 4, lines 29-36 and Fig. 4B). Therefore, it would have been obvious to one of ordinary skill in the art to couple a fourth transistor between third transistor 16 of Hardee and ground. This fourth transistor would have a thin gate insulation layer because it is related to the lower voltages within the device, not high voltage VCCP. Therefore, claim 17 is rendered obvious. The fourth transistor would provide another means for dropping voltage, thus helping to distribute the total voltage drop between the output terminal and ground across more transistors. Also, if the fourth transistor is used as part of a NAND logic configuration, it is capable of receiving a block selecting signal from the memory device, rendering obvious claim 18. Configured as NAND logic, the device will provide a low output signal only when the second input signal, and the block selecting signal, allow the third and fourth transistors to conduct. This will help ensure that the device will

generate a low only when these specific conditions are met, and only when a low output signal is actually desired. By re-identifying the restricting means of claim 1 as an interface circuit, claims 32-33 and 35 are rendered obvious for the same type of reasoning as previously described above with respect to claims 1-2. [However, it is noted that since independent claim 32 does not cite an inverter and its transistors. Therefore, they do not have to be considered with respect to claims 32-3 and 35-37.] Since third MOS transistor 14 functions as a resistance device, one of ordinary skill in the art would know that it prevents first voltage VCCP from being directly applied to the drain of second MOS transistor 16, thus enabling it to have the thin gate insulation layer, and reducing the gate-drain voltage of second MOS transistor 16 to alleviate the electric field applied to the gate insulation layer of second MOS transistor 16. This knowledge renders respective claims 36 and 37 obvious.

Claims 4-9, 14-15, 25, 27-28, and 34 have been cancelled.

Allowable Subject Matter

Claims 19-24, 26, and 29-31 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the devices comprises the first-sixth MOS transistors cited within claim 19, as well as the first internal node being coupled to a row decoder and driver block of the memory device, wherein that block selectively drives word lines of the memory device in response to a row address signal. Claims 20-24, 26 and 29-31 depend upon claim 19.

Response to Arguments

The applicant's arguments, see the amendment filed Apr 24, 2008, with respect to the rejection(s) of claim(s) 1-3, 10-13, and 16-18 under 35 U.S.C. 103(a) (with respect to Hardee/ Amanai) have been fully considered and are persuasive, up to a point. Therefore, the rejection

has been withdrawn. However, upon further consideration, a new (i.e. modified) ground(s) of rejection is made in view Hardee/Amanai, with the addition of a reference by Wang et al., which was previously cited on paper 20070109. The Wang et al. reference provides an example of an inverter with PMOS and NMOS transistors, each having a thick gate insulation layer.

In response to the applicant's apparent argument that the references fail to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (i.e., an inverter with transistors having thick gate insulation layers) are not recited in rejected claims 32-33 and 35-37. For example, independent claim 32 does not even cite an inverter. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln D. Donovan, can be reached on (571) 272-1988

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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/T.L.E./

Examiner, Art Unit 2816

/Lincoln Donovan/

Supervisory Patent Examiner, Art Unit 2816